Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **V +**
2. **V-**
3. **ADJ**

**.045”**

**.045”**

**1**

**3**

**2**

**MASK**

**REF**

**136B**

**B**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .045” X .047” DATE: 10/20/21**

**MFG: NATIONAL SEMI THICKNESS .015” P/N: LM136-5.0**

**DG 10.1.2**

#### Rev B, 7/19/02